# DRV5053 Analog-Bipolar Hall Effect Sensor

## 1 Features

- Linear Output Hall Sensor
- Superior Temperature Stability
  - Sensitivity ±10% Over Temperature
- High Sensitivity Options:
  - –10 mV/mT (OA)
  - –20 mV/mT (PA)
  - –40 mV/mT (RA)
  - –80 mV/mT (VA)
  - +20 mV/mT (CA)
  - +40 mV/mT (EA)
- Supports a Wide Voltage Range
  - 2.5 to 38 V
  - Operation from Unregulated Supply
- Wide Operating Temperature Range
  - $T_A$ = –40 to 125°C (Q)
- Amplified Output Stage
  - 2.3-mA Sink, 300 µA Source
- Output voltage: 0.2 ~ 1.8 V
  - B = 0 mT, OUT = 1.0 V
- Fast Power-On: 35 µs
- Small Package and Footprint
  - Surface Mount 3-Pin SOT-23 (DBZ)
    - 2.92 mm × 2.37 mm
  - Through-Hole 3-Pin SIP (LPG)
    - 4.00 mm × 3.15 mm
- **Protection Features**
  - Reverse Supply Protection (up to –22 V)
  - Supports up to 40-V Load Dump
  - Output Short-Circuit Protection
  - Output Current Limitation

## 2 Applications

- Flow Meters
- Docking Adjustment
- Vibration Correction
- Damper Controls

## 3 Description

The DRV5053 device is a chopper-stabilized Hall IC that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

The 0 V to 2 V analog output responds linearly to the applied magnetic flux density, and distinguishes the polarity of magnetic field direction. A wide operating voltage range from 2.5 V to 38 V with reverse polarity protection up to –22V makes the device suitable for a wide range of industrial and consumer applications.

Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or overcurrent.

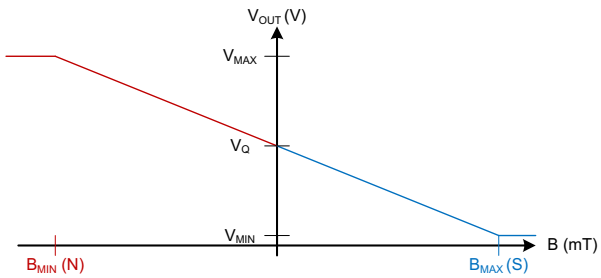
**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DRV5053 | SOT-23 (3) | 2.92mm × 2.37mm |
| | SIP (3) | 4.00mm × 3.15mm |

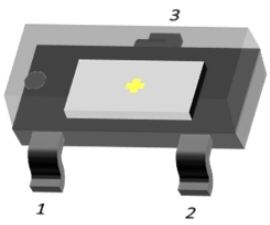
(1) For all available packages, see the orderable addendum at the end of the data sheet.

PRODUCT PREVIEW

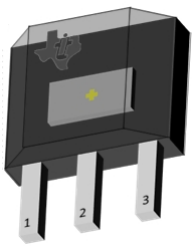
## 4 Output State




SOT-23




SIP



# Table of Contents



PRODUCT PREVIEW

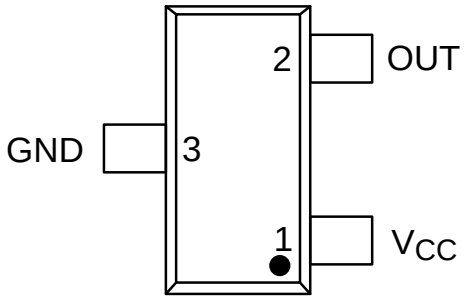
## 5 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| May 2014 | * | Initial release. |

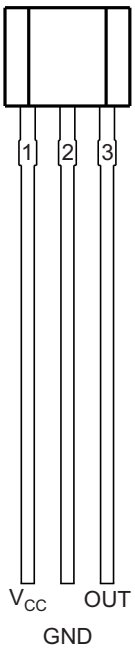
## 6 Pin Configuration and Functions

For additional configuration information, see and Mechanical, Packaging, and Orderable Information.

**3-Pin SOT-23**
**DBZ Package**
**(Top View)**




**3-Pin SIP**
**LPG Package**
**(Top View)**




**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NUMBER | | | |
| | DBZ | LPG | | |
| GND | 3 | 2 | GND | Ground pin |
| VCC | 1 | 1 | Power | 2.5 to 38 V power supply. Bypass this pin to the GND pin with a 0.01-µF (minimum) ceramic capacitor rated for $V_{CC}$. |
| OUT | 2 | 3 | Output | Hall sensor analog output. 1.0 V output corresponds to B = 0 mT |

PRODUCT PREVIEW

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | –22(2) | 40 | V |
| | Voltage ramp rate ($V_{CC}$), $V_{CC}$ < 5 V | Unlimited | | V/µs |
| | Voltage ramp rate ($V_{CC}$), $V_{CC}$ > 5 V | 0 | 2 | |
| Output pin voltage | OUT | –0.5 | 2.5 | V |
| Output pin reverse current during reverse supply condition | OUT | 0 | –20 | mA |
| Operating junction temperature | $T_J$ | –40 | 175(3) | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Ensured by design. Only tested to –20 V.
(3) Tested in production to $T_A$ = 125°C.

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | –2.5 | 2.5 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | –500 | 500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | 2.5 | 38 | V |
| $V_{OUT}$ | Output pin voltage (OUT) | 0 | 2 | V |
| $I_{SOURCE}$ | Output pin current source (OUT) | 0 | 300 | µA |
| $I_{SINK}$ | Output pin current sink (OUT) | 0 | 2.3 | mA |
| $T_A$ | Operating ambient temperature | –40 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | DBZ (3 PINS) | LPG (3 PINS) | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 333.2 | 180 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 99.9 | 98.6 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 66.9 | 154.9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.9 | 40 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 65.2 | 154.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES ($V_{CC}$)** | | | | | | |
| $V_{CC}$ | $V_{CC}$ operating voltage | | 2.5 | | 38 | V |
| $I_{CC}$ | Operating supply current | $V_{CC}$ = 2.5 to 38 V, $T_A$ = 25°C | | 2.7 | | mA |
| | | $V_{CC}$ = 2.5 to 38 V, $T_A$ = 125°C | | 3 | 3.5 | |
| $t_{on}$ | Power-on time | | | 35 | 50 | µs |
| **PROTECTION CIRCUITS** | | | | | | |
| $V_{CCR}$ | Reverse supply voltage | | –22 | | | V |
| $I_{OCP,SOURCE}$ | Overcurrent protection level | Sourcing current | | 300 | | µA |
| $I_{OCP,SINK}$ | Overcurrent protection level | Sinking current | | 2.3 | | mA |

## 7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPEN DRAIN OUTPUT (OUT)** | | | | | | |
| $t_d$ | Output delay time | | | 13 | 25 | µs |

## 7.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT(1) |
|---|---|---|---|---|---|---|
| $V_Q$ | Quiescent output | B = 0 mT<br>$T_A$ = –40°C to +125°C | 0.9 | 1.0 | 1.1 | V |
| $f_{BW}$ | Output bandwidth | 3 dB point | 20 | | | kHz |
| $B_N$ | Input-referred noise(2) | $C_{OUT}$ = 50 pF<br>$T_A$ = –40°C to +125°C | 0.40 | 0.57 | 0.79 | $mT_{pp}$ |
| Le | Linearity | $–B_{SAT} < B < B_{SAT}$ | | 1 | | % |
| $V_{OUT\ MIN}$ | Output saturation voltage (min) | $B < –B_{SAT}$ | | | 0.2 | V |
| $V_{OUT\ MAX}$ | Output saturation voltage (max) | $B > B_{SAT}$ | 1.8 | | | V |
| **DRV5053OA: –10 mV/mT** | | | | | | |
| S | Sensitivity | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | –5 | –10 | –17.5 | mV/mT |
| $V_N$ | Output-referred noise(2) | VCC = 3.3 V; $R_{OUT}$ = 10 kΩ;<br>$C_{OUT}$ = 50 pF<br>$T_A$ = –40°C ~ +125°C | | 6 | | $mV_{pp}$ |
| $B_{SAT}$ | Input saturation field | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | | 80 | | mT |
| **DRV5053PA: –20 mV/mT** | | | | | | |
| S | Sensitivity | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | –10 | –20 | –35 | mV/mT |
| $V_N$ | Output-referred noise(2) | VCC = 3.3 V; $R_{OUT}$ = 10 kΩ;<br>$C_{OUT}$ = 50 pF<br>$T_A$ = –40°C ~ +125°C | | 13 | | $mV_{pp}$ |
| $B_{SAT}$ | Input saturation field | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | | 40 | | mT |

(1) 1 mT = 10 Gauss
(2) Not tested in production; limits are based on characterization data.

PRODUCT PREVIEW

## Magnetic Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT(1) |
|---|---|---|---|---|---|---|
| **DRV5053RA: –40 mV/mT** | | | | | | |
| S | Sensitivity | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | –20 | –45 | –70 | mV/mT |
| $V_N$ | Output-referred noise(3) | VCC = 3.3 V; $R_{OUT}$ = 10 kΩ;<br>$C_{OUT}$ = 50 pF<br>$T_A$ = –40°C ~ +125°C | 17 | 26 | 37 | $mV_{pp}$ |
| $B_{SAT}$ | Input saturation field | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | | 18 | | mT |
| **DRV5053VA: –80 mV/mT** | | | | | | |
| S | Sensitivity | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | –35 | –80 | –140 | mV/mT |
| $V_N$ | Output-referred noise(3) | VCC = 3.3 V; $R_{OUT}$ = 10 kΩ;<br>$C_{OUT}$ = 50 pF<br>$T_A$ = –40°C ~ +125°C | | 52 | | $mV_{pp}$ |
| $B_{SAT}$ | Input saturation field | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | | 10 | | mT |
| **DRV5053CA: +20 mV/mT** | | | | | | |
| S | Sensitivity | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | 10 | +20 | 35 | mV/mT |
| $V_N$ | Output-referred noise(3) | VCC = 3.3 V; $R_{OUT}$ = 10 kΩ;<br>$C_{OUT}$ = 50 pF<br>$T_A$ = –40°C ~ +125°C | | 13 | | $mV_{pp}$ |
| $B_{SAT}$ | Input saturation field | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | | 40 | | mT |
| **DRV5053EA: +40 mV/mT** | | | | | | |
| S | Sensitivity | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | +20 | +45 | +70 | mV/mT |
| $V_N$ | Output-referred noise(3) | VCC = 3.3 V; $R_{OUT}$ = 10 kΩ;<br>$C_{OUT}$ = 50 pF<br>$T_A$ = –40°C ~ +125°C | 17 | 26 | 37 | $mV_{pp}$ |
| $B_{SAT}$ | Input saturation field | VCC = 3.3 V<br>$T_A$ = –40°C ~ +125°C | | 18 | | mT |

(3) Not tested in production; limits are based on characterization data.

PRODUCT PREVIEW

## 7.8 Typical Characteristics

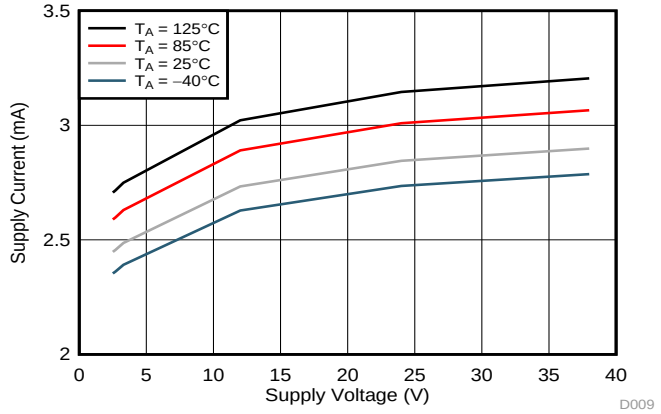



**Figure 1. $I_{CC}$ vs $V_{CC}$**

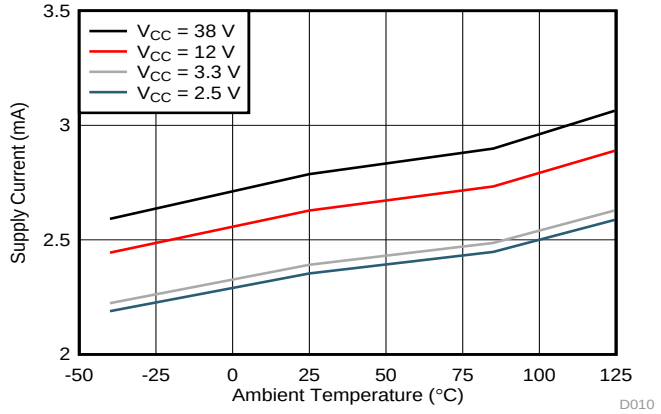



**Figure 2. $I_{CC}$ vs Temperature**

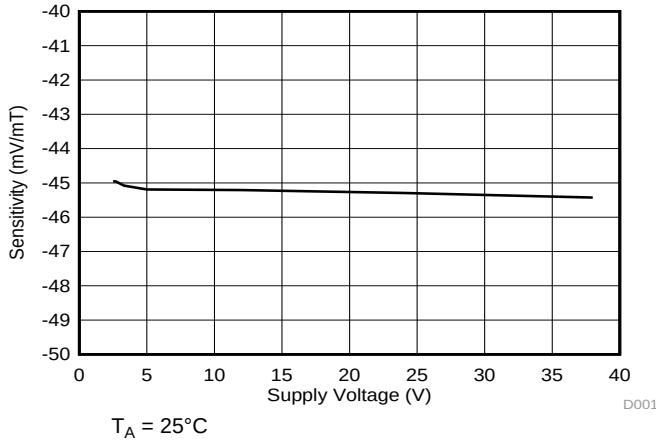



**Figure 3. DRV5053AD Sensitivity vs $V_{CC}$**

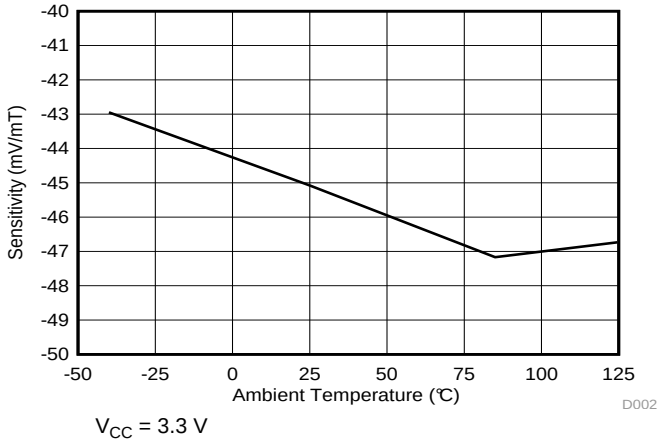



**Figure 4. DRV5053AD Sensitivity vs Temperature**

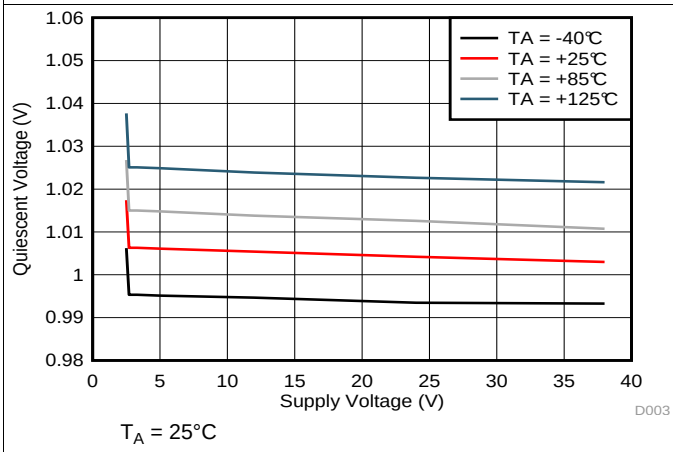



**Figure 5. DRV5053AD $V_Q$ vs $V_{CC}$**

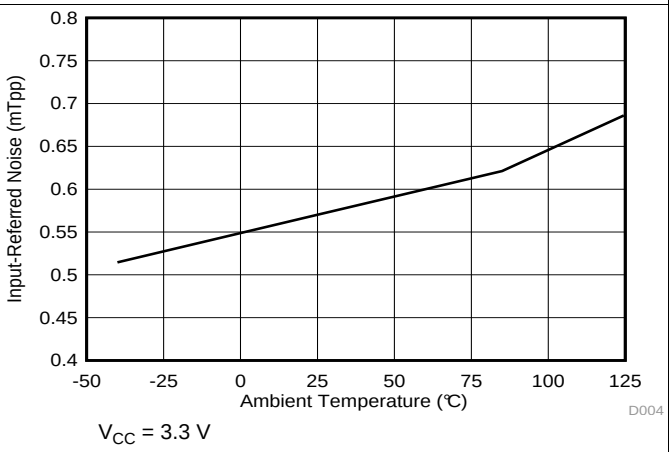



**Figure 6. DRV5053AD $B_N$ vs Temperature**

PRODUCT PREVIEW

# 8 Detailed Description

## 8.1 Output Change

The DRV5053 device is a chopper-stabilized hall sensor with an analog output for magnetic sensing applications. The DRV5053 device can be powered with a supply voltage between 2.5 and 38 V, and will survive –22 V reverse battery conditions continuously. Note that the DRV5053 device will not be operating when –22 ~ 2.4 V is applied to VCC (with respect to GND). In addition, the device can withstand supply voltages up to 40 V for transient durations.

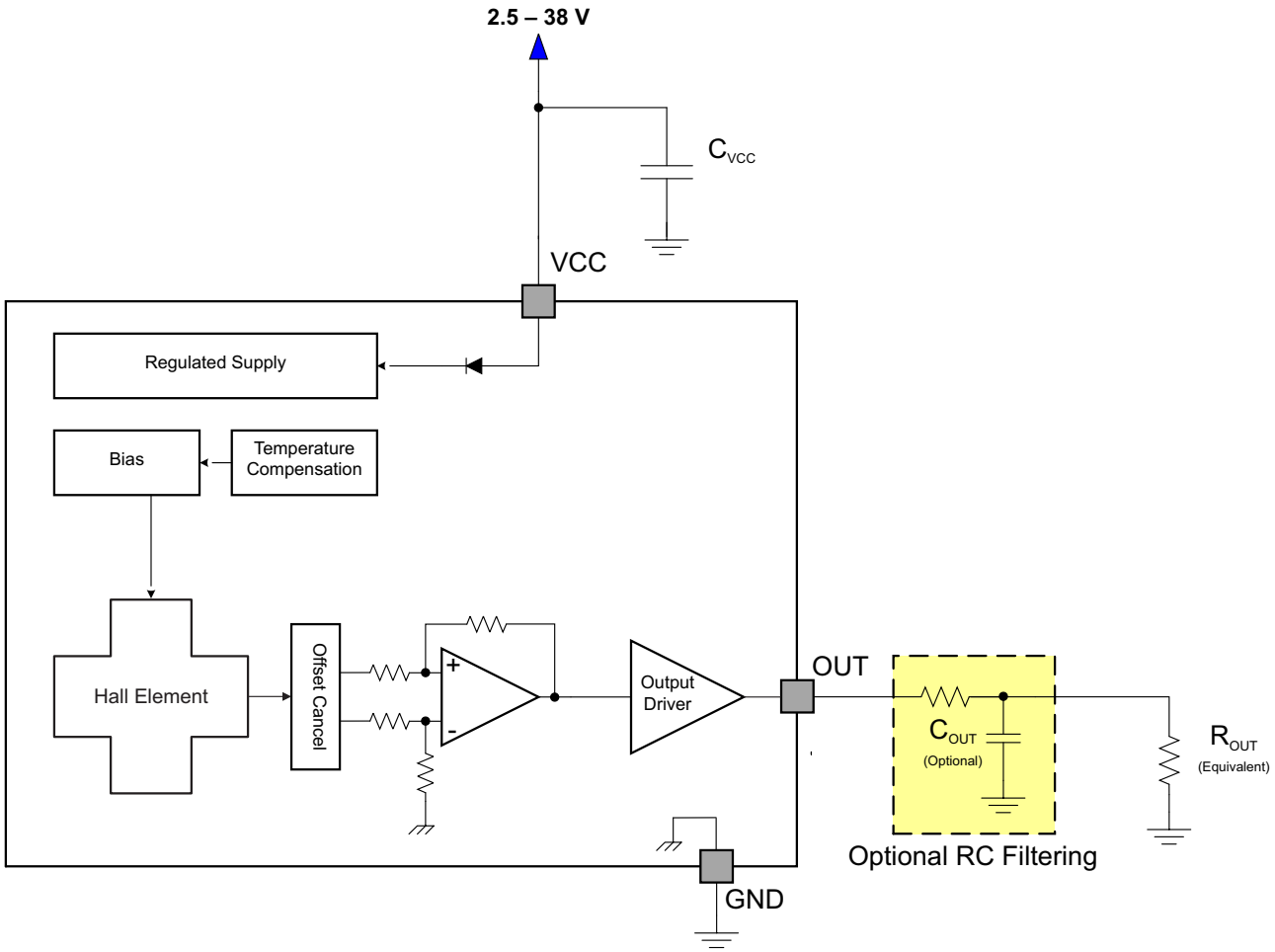
The output voltage is dependent on the magnetic field perpendicular to the package. The absence of a magnetic field will result in OUT = 1.0 V. A magnetic field will cause the output voltage to change linearly with the magnetic field.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

For devices with a negative sensitivity (that is, DRV5053RA: –40 mV/mT), a south pole will cause the output voltage to drop below 1.0 V, and a north pole will cause the output to rise above 1.0 V.

For devices with a positive sensitivity (that is, DRV5053EA: +40 mV/mT), a south pole will cause the output voltage to rise above 1.0 V, and a north pole will cause the output to drop below 1.0 V.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 7.

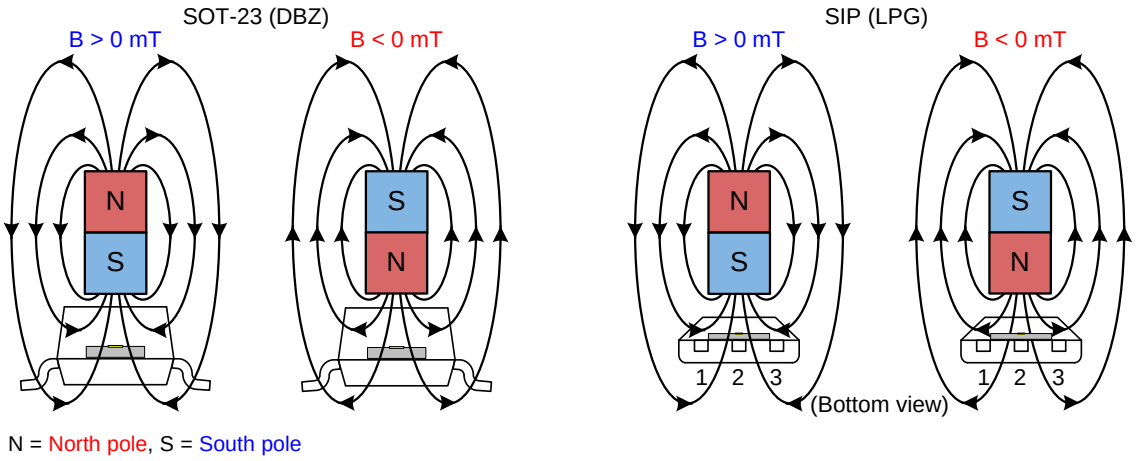



**Figure 7. Field Direction Definition**

### 8.3.2 Device Output

The DRV5053 device output is defined below for negative sensitivity (that is, –40 mV/mT, RA) and positive sensitivity (that is, +40 mV/mT, EA):

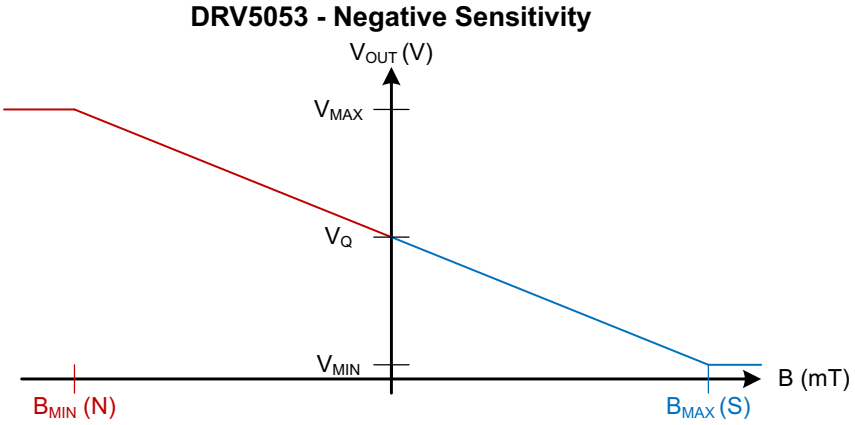



**Figure 8. DRV5053—Negative Sensitivity**

PRODUCT PREVIEW

## Feature Description (continued)

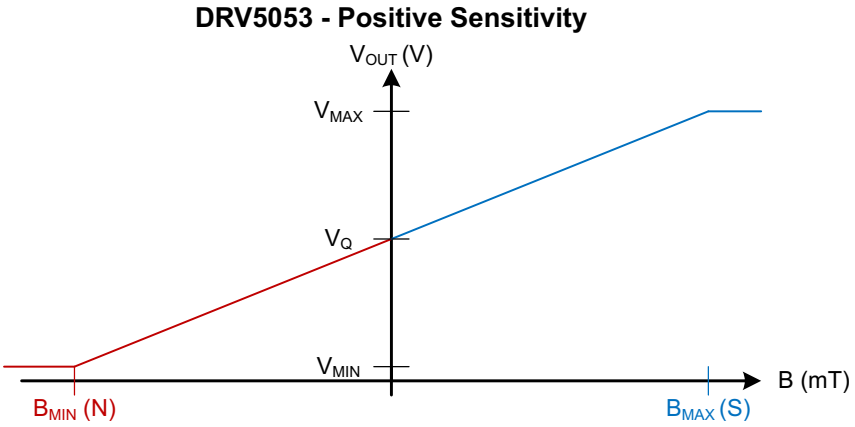



**Figure 9. DRV5053—Positive Sensitivity**

PRODUCT PREVIEW

## Feature Description (continued)

### 8.3.3 Power-On Time

After applying $V_{CC}$ to the DRV5053 device, $t_{on}$ must elapse before OUT is valid. Figure 10 shows Case 1 and Figure 11 shows Case 2; the output is defined assuming a negative sensitivity device and a constant magnetic field $–B_{SAT} < B < B_{SAT}$.

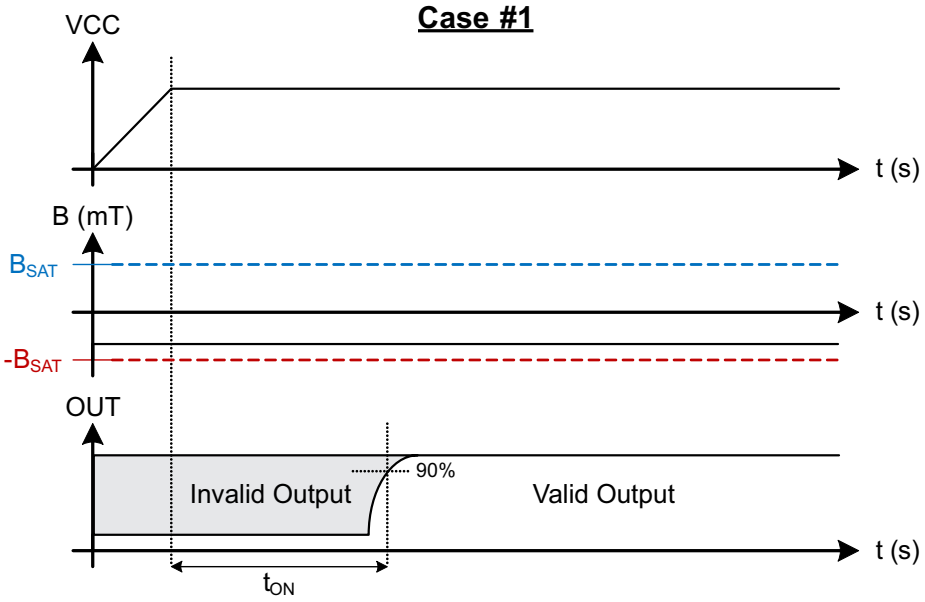



**Figure 10. Case 1: Power On When B < 0, North**

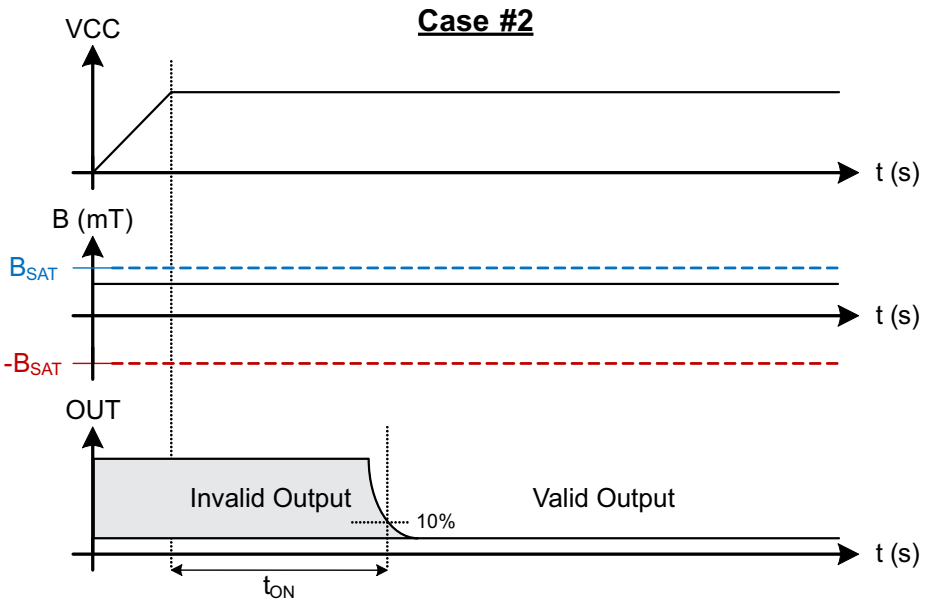



**Figure 11. Case 2: Power On When B > 0, South**

PRODUCT PREVIEW

## Feature Description (continued)

### 8.3.4 Output Stage

The DRV5053 output stage is capable of up to 300 µA of current source or 2.3 mA sink.

For proper operation, ensure that equivalent output load ROUT > 10 kΩ. In addition, ensure that the load capacitance $C_{OUT}$ < 10 nF.

### 8.3.5 Protection Circuits

An analog current limit circuit limits the current through the output driver. The driver current will be clamped to $I_{OCP}$

#### *8.3.5.1 Overcurrent Protection (OCP)*

An analog current-limit circuit limits the current through the FET. The driver current is clamped to $I_{OCP}$. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

#### *8.3.5.2 Load Dump Protection*

The DRV5053 device operates at DC $V_{CC}$ conditions up to 38 V nominally, and can additionally withstand $V_{CC}$ = 40 V. No current-limiting series resistor is required for this protection.

#### *8.3.5.3 Reverse Supply Protection*

The DRV5053 device is protected in the event that the $V_{CC}$ pin and the GND pin are reversed (up to –22 V).

**NOTE**

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the Absolute Maximum Ratings.

| FAULT | CONDITION | DEVICE | DESCRIPTION | RECOVERY |
|---|---|---|---|---|
| FET overload (OCP) | $I_{SINK} \geq I_{OCP}$ | Operating | Output current is clamped to $I_{OCP}$ | $I_O < I_{OCP}$ |
| Load Dump | 38 V < $V_{CC}$ < 40 V | Operating | Device will operate for a transient duration | $V_{CC} \leq$ 38 V |
| Reverse Supply | –22 V < $V_{CC}$ < 0 V | Disabled | Device will survive this condition | $V_{CC} \geq$ 2.5 V |

## 8.4 Device Functional Modes

The DRV5053 device is active only when $V_{CC}$ is between 2.5 and 38 V.

When a reverse supply condition exists, the device is inactive.

PRODUCT PREVIEW

# 9 Application and Implementation

## 9.1 Application Information

The DRV5053 device is used in magnetic-field sensing applications.

## 9.2 Typical Application

### 9.2.1 Application With No Filter

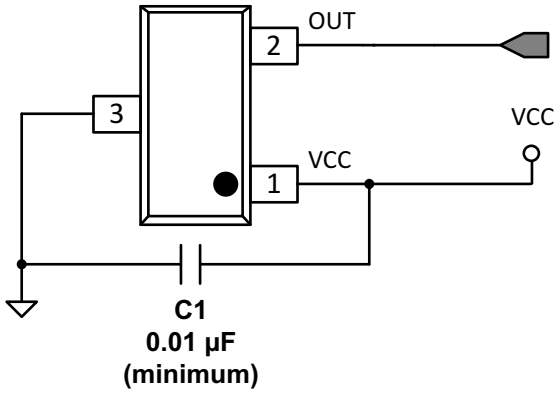



**Figure 12. Typical Application Circuit**

#### *9.2.1.1 Design Requirements*

For this design example, use the parameters listed in Table 1 as the input parameters.

**Table 1. Design Parameters**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| System bandwidth | $f_{BW}$ | 15 kHz |

#### *9.2.1.2 Detailed Design Procedure*

The DRV5053 has internal filtering that limits the bandwidth to at least 20 kHz. For this application no external components are required other than the C1 bypass capacitor, which is 0.01 µF minimum. If the analog output OUT is tied to a microcontroller ADC input, the equivalent load must be R > 10 kΩ and C < 10 nF.

**Table 2. External Components**

| COMPONENT | PIN 1 | PIN 2 | RECOMMENDED |
|---|---|---|---|
| C1 | $V_{CC}$ | GND | A 0.01-µF (minimum) ceramic capacitor rated for $V_{CC}$ |

PRODUCT PREVIEW

#### 9.2.1.3 Application Curves

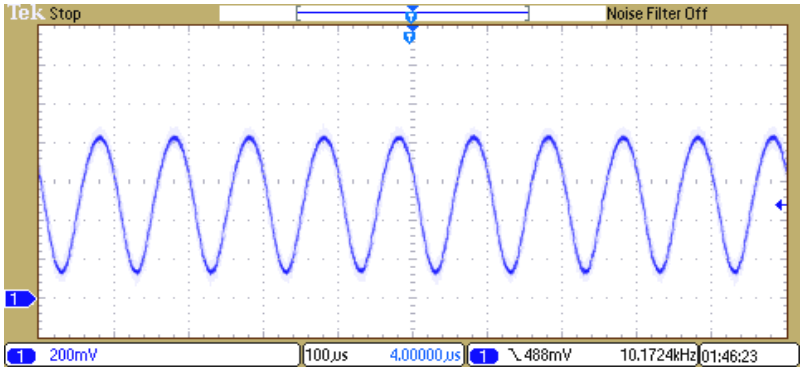



**Figure 13. 10-kHz Switching Magnetic Field**

### 9.2.2 Filtered Application

For lower noise on the analog output OUT, additional RC filtering can be added to further reduce the bandwidth.

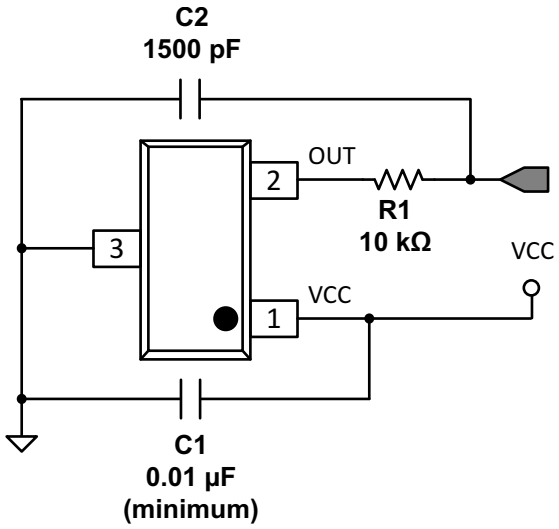



**Figure 14. Typical Application Circuit**

#### 9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

**Table 3. Design Parameters**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| System bandwidth | $f_{BW}$ | 5 kHz |

#### 9.2.2.2 Detailed Design Procedure

In this example we will add an external RC filter in order to reduce the output bandwidth.

In order to preserve the signal at the frequencies of interest, we will conservatively select a low-pass filter bandwidth (–3 dB point) at twice the system bandwidth (10 kHz).

$$10\ \text{kHz} < \frac{1}{2\pi \times R_1 \times C_2} \tag{1}$$

If we guess R1 = 10 kΩ, then C2 < 1590 pF. So we select C2 = 1500 pF.

#### 9.2.2.3 Application Curves

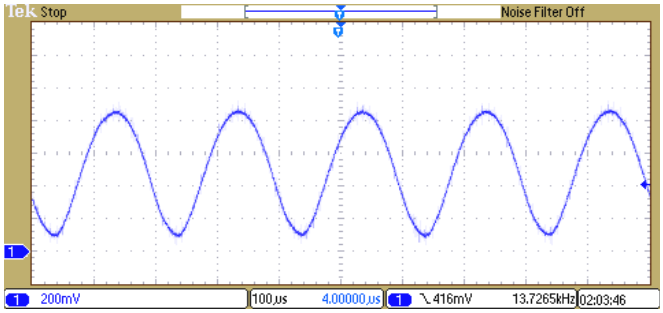
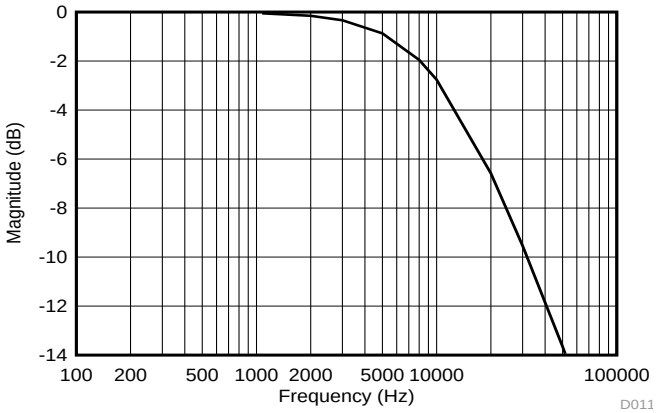



**Figure 15. 5-kHz Switching Magnetic Field**




R1 = 10-kΩ pullup C2 = 680 pF

**Figure 16. Low-Pass Filtering**

## 10 Power Supply Recommendations

The DRV5053 device is designed to operate from an input voltage supply (VM) range between 2.5 V and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for $V_{CC}$ must be placed as close to the DRV5053 device as possible.

PRODUCT PREVIEW

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Device Nomenclature

Figure 17 shows a legend for reading the complete device name for and DRV5053 device.

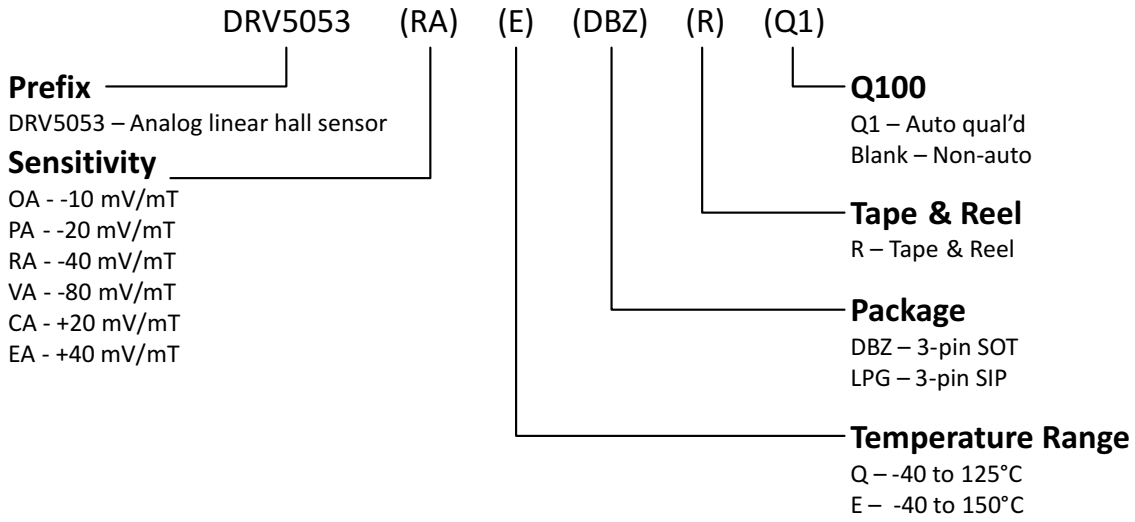



**Figure 17. Device Nomenclature**

### 11.1.2 Device Markings

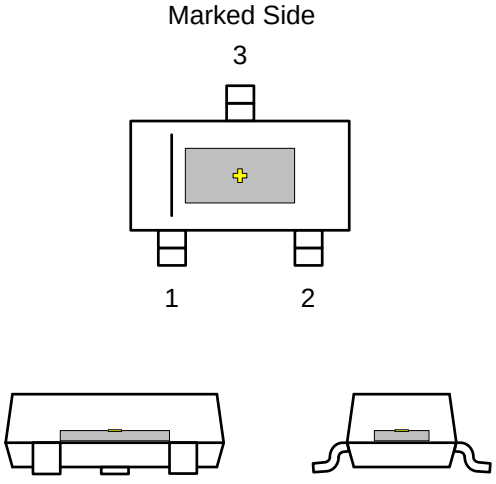



**Figure 18. SOT-23 (DBZ) Package**

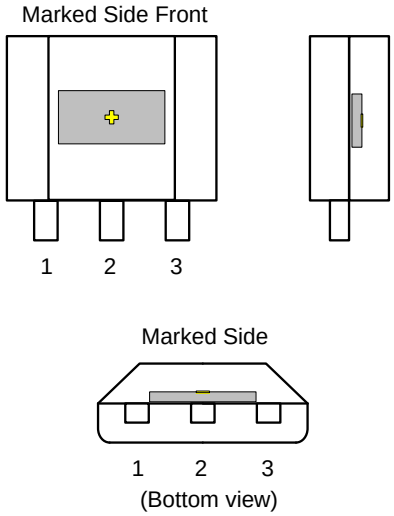



**Figure 19. SIP (LPG) Package**

✚ indicates the Hall Effect Sensor (not to scale). Located in the center of the package.

PRODUCT PREVIEW

### 11.2 Trademarks

All trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV5053CAQDBZR | PREVIEW | SOT-23 | DBZ | 3 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053CAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053EAQDBZR | PREVIEW | SOT-23 | DBZ | 3 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053EAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053OAQDBZR | PREVIEW | SOT-23 | DBZ | 3 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053OAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053PAQDBZR | PREVIEW | SOT-23 | DBZ | 3 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053PAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053RAQDBZR | PREVIEW | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | | |
| DRV5053RAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053VAQDBZR | PREVIEW | SOT-23 | DBZ | 3 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| DRV5053VAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053CAQDBZT | PREVIEW | SOT-23 | DBZ | 3 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053CAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053EAQDBZT | PREVIEW | SOT-23 | DBZ | 3 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053EAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053OAQDBZT | PREVIEW | SOT-23 | DBZ | 3 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053OAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053PAQDBZT | PREVIEW | SOT-23 | DBZ | 3 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053PAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053RAQDBZT | PREVIEW | SOT-23 | DBZ | 3 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053RAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053VAQDBZT | PREVIEW | SOT-23 | DBZ | 3 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV5053VAQLPG | PREVIEW | TO-92 | LPG | 3 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

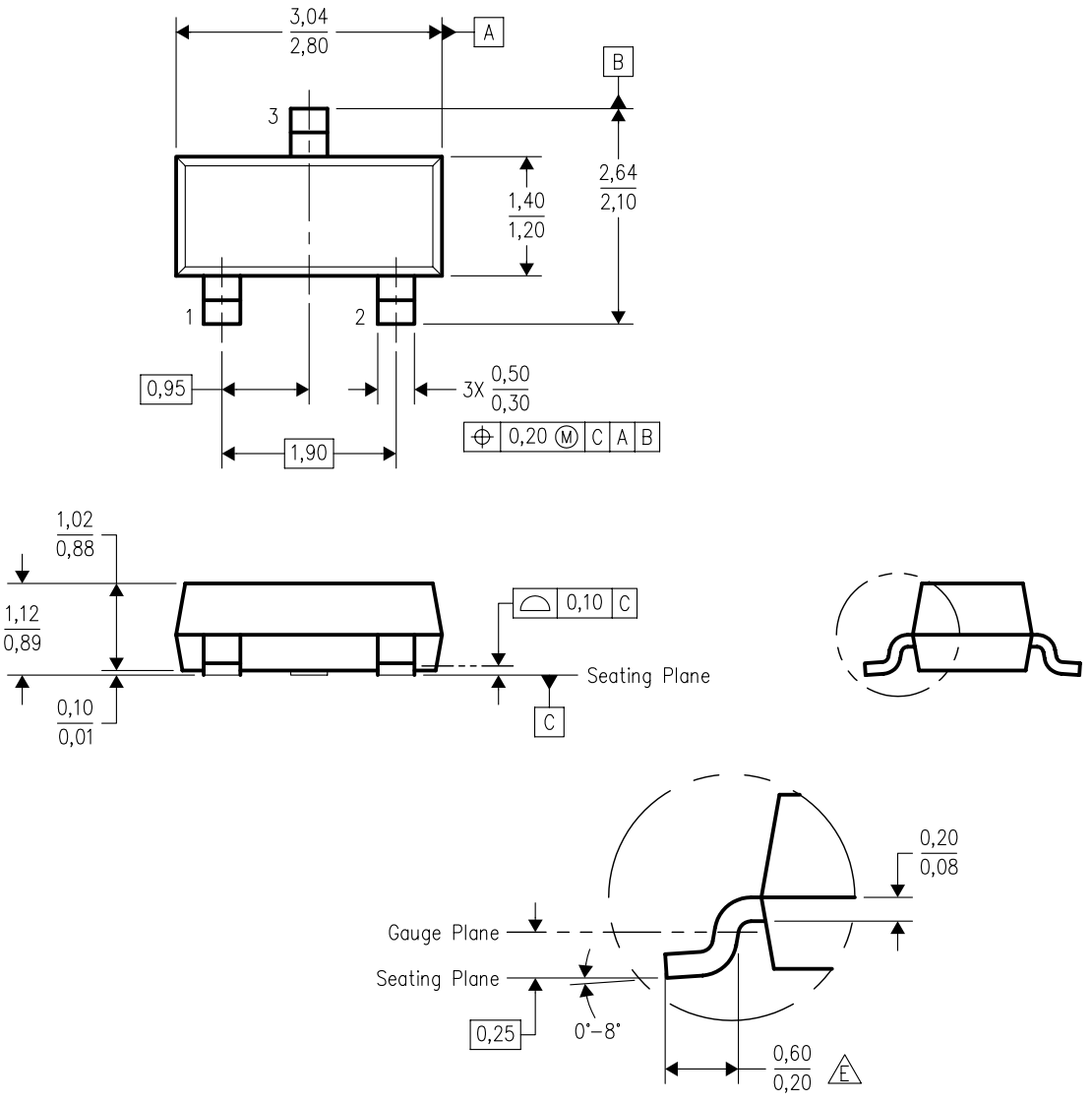
**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## DBZ (R–PDSO–G3) PLASTIC SMALL–OUTLINE



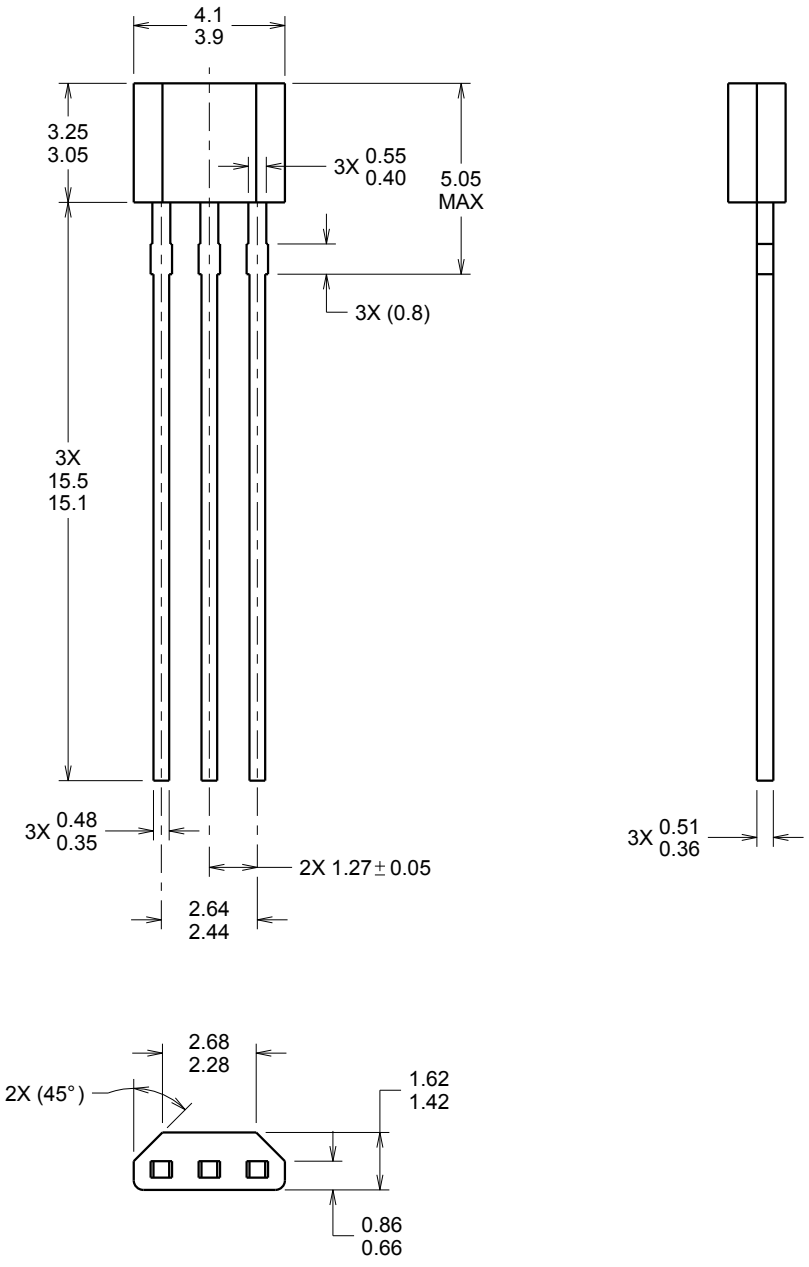

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Lead dimensions are inclusive of plating.
D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
E. Falls within JEDEC TO–236 variation AB, except minimum foot length.

# PACKAGE OUTLINE

## LPG0003A

## TO-92 - 5.05 mm max height

TO-92




4221343/A 02/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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